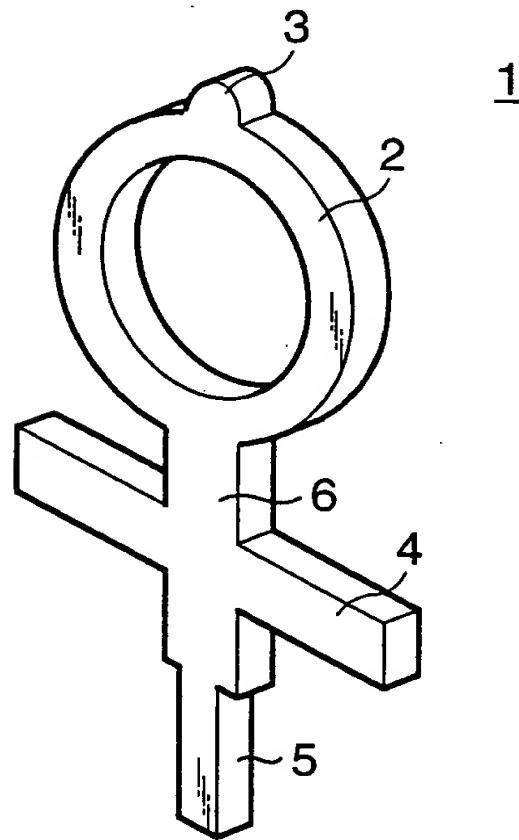




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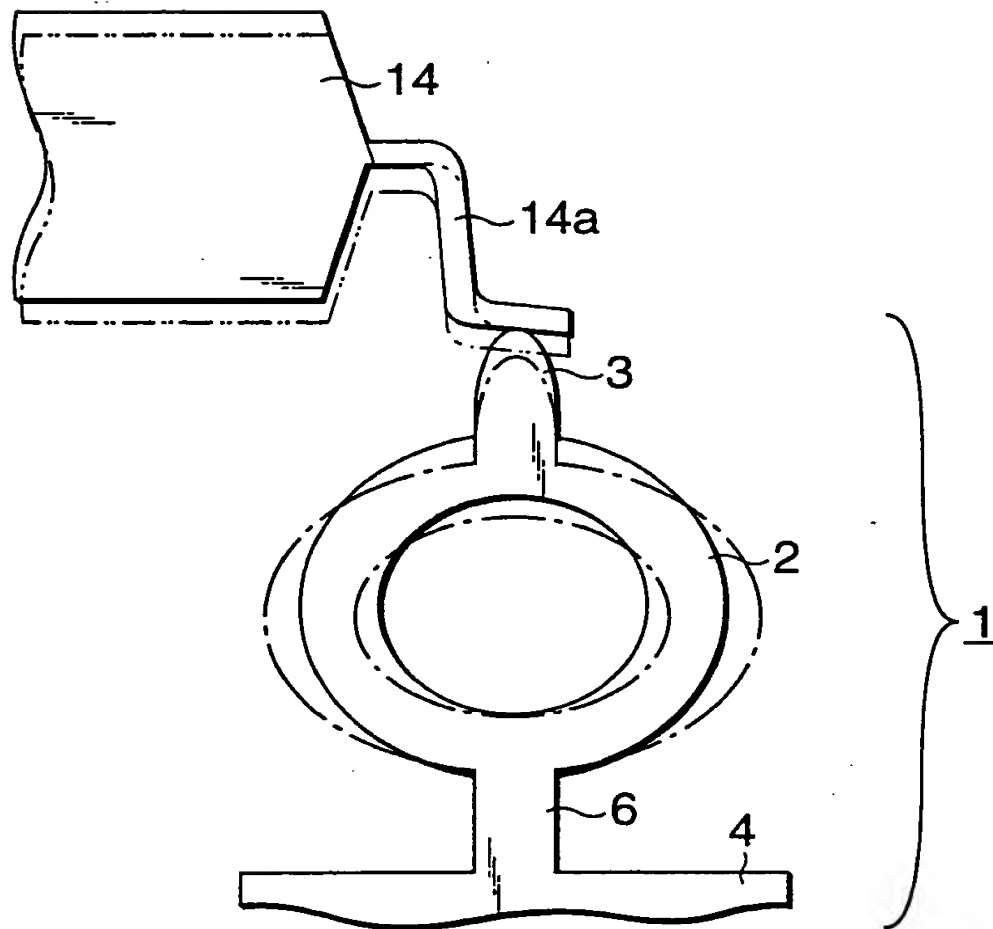
FIG.1





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FIG.2



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FIG.3

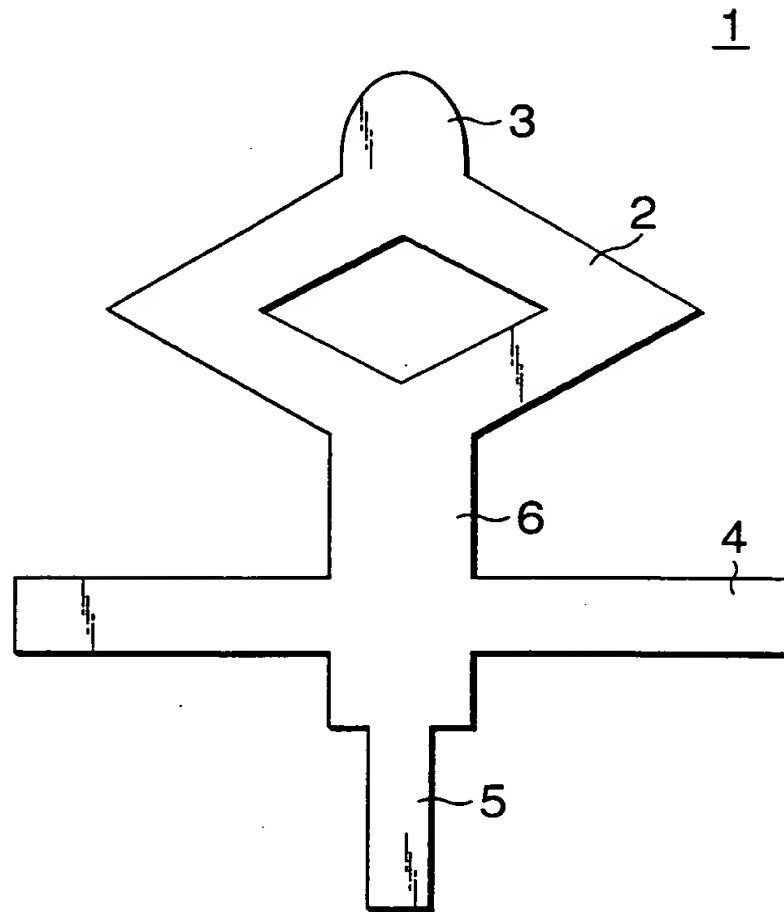
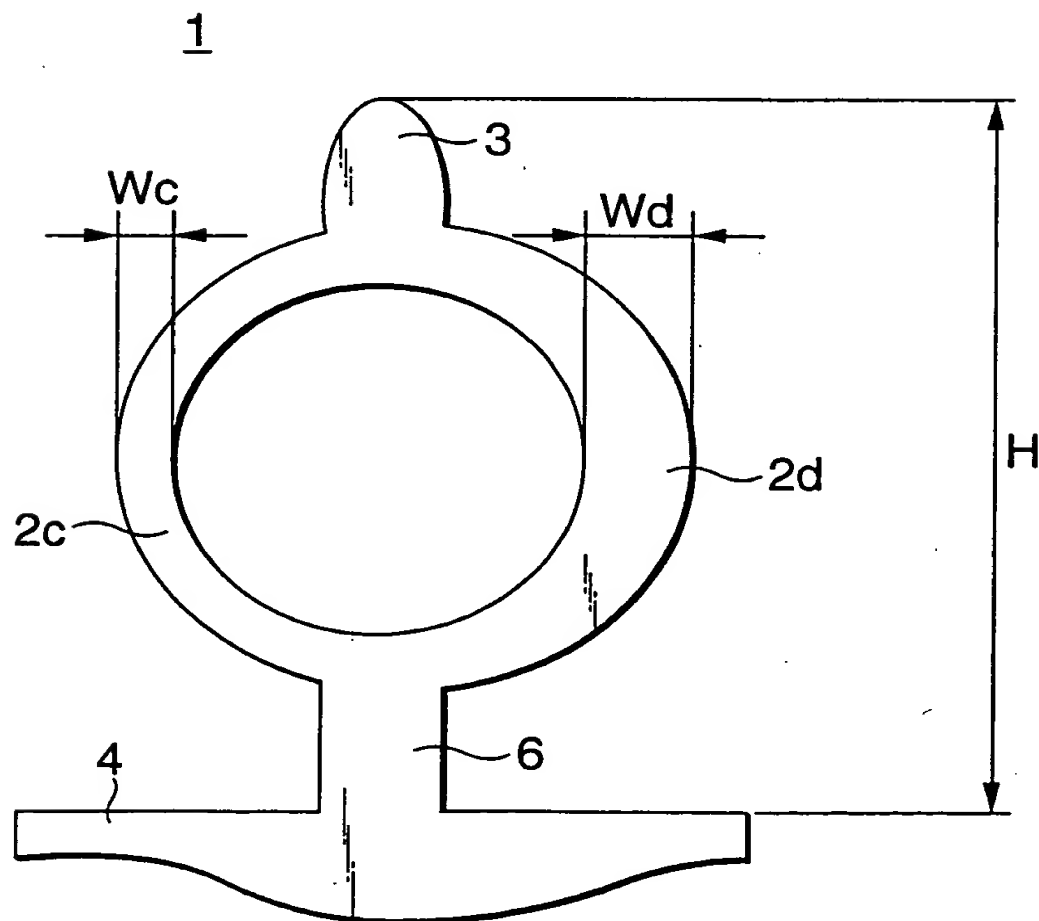


FIG.4





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FIG.5

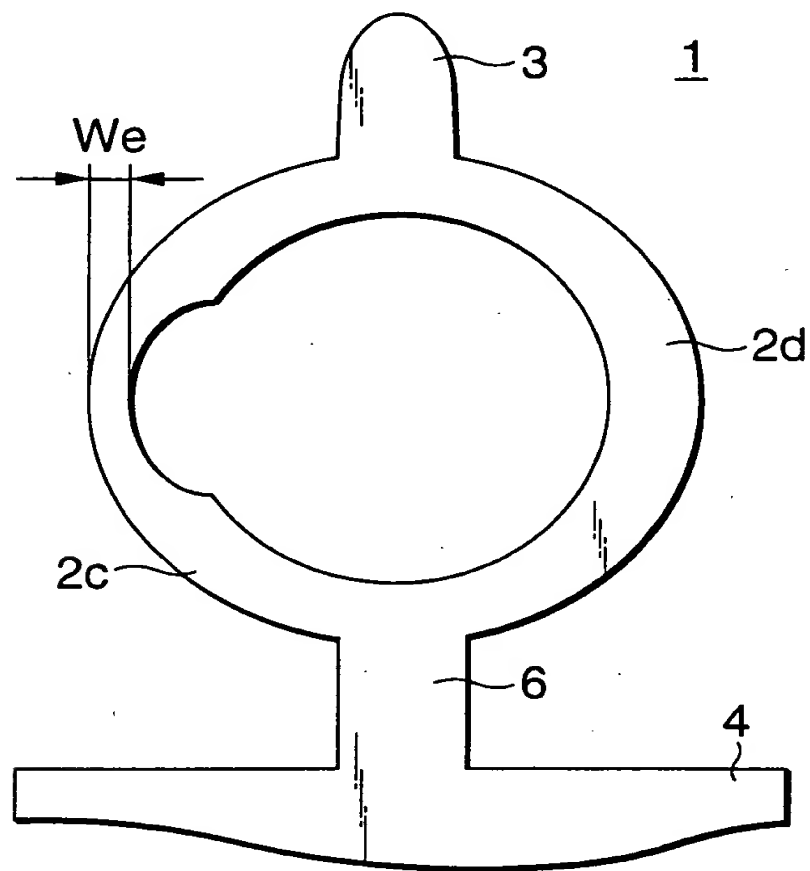
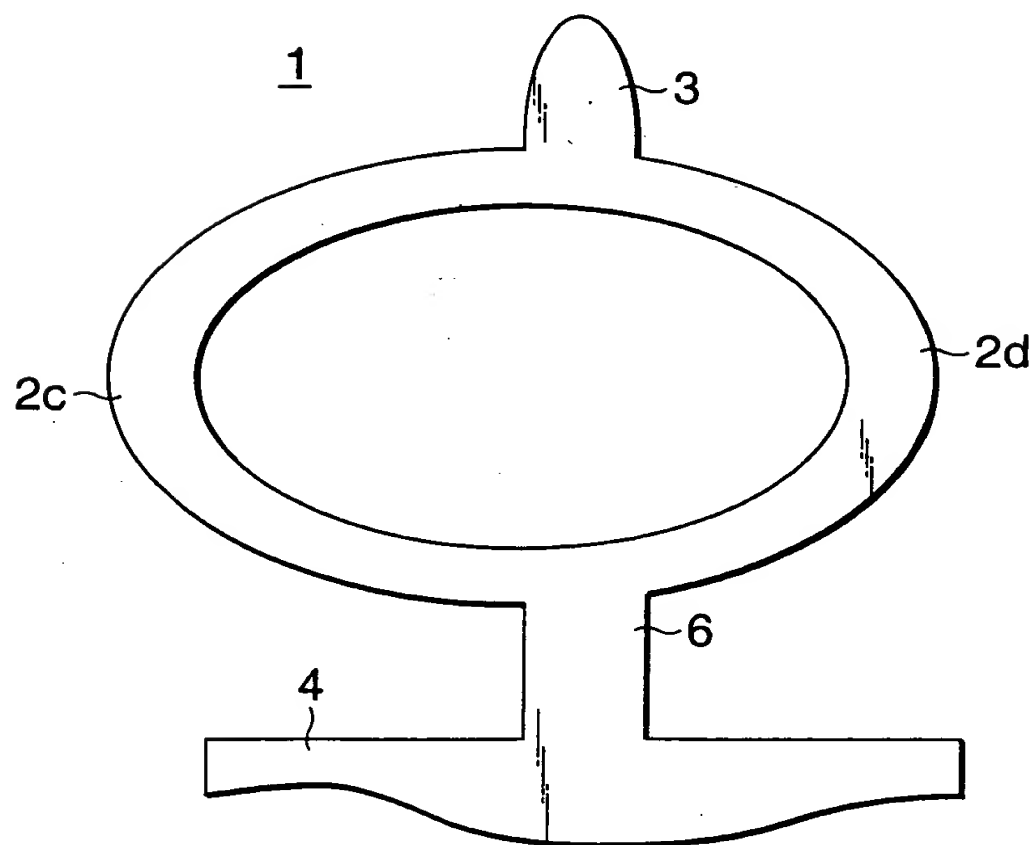


FIG.6





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FIG.7

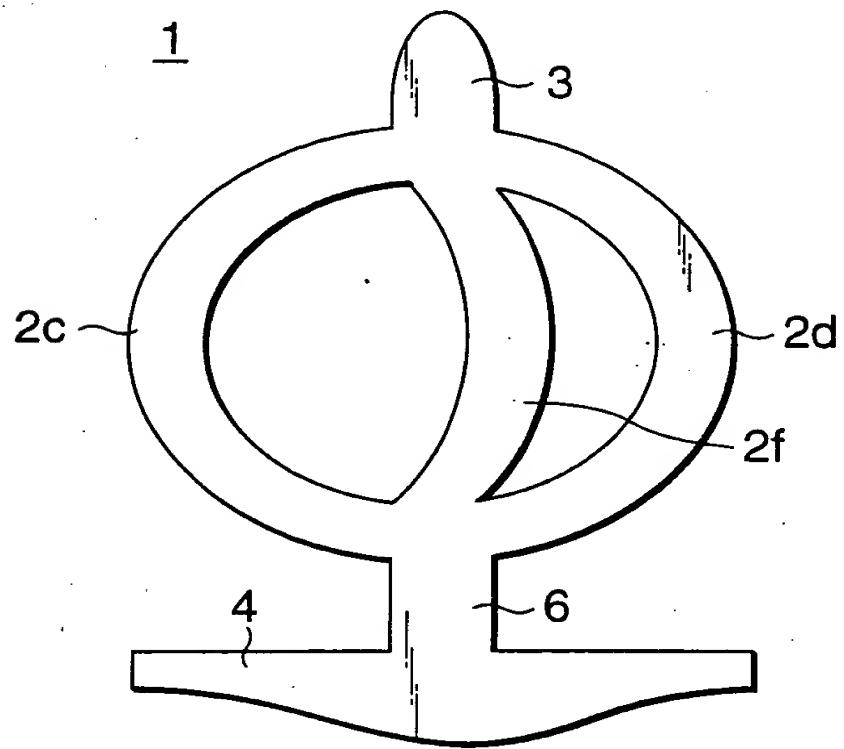
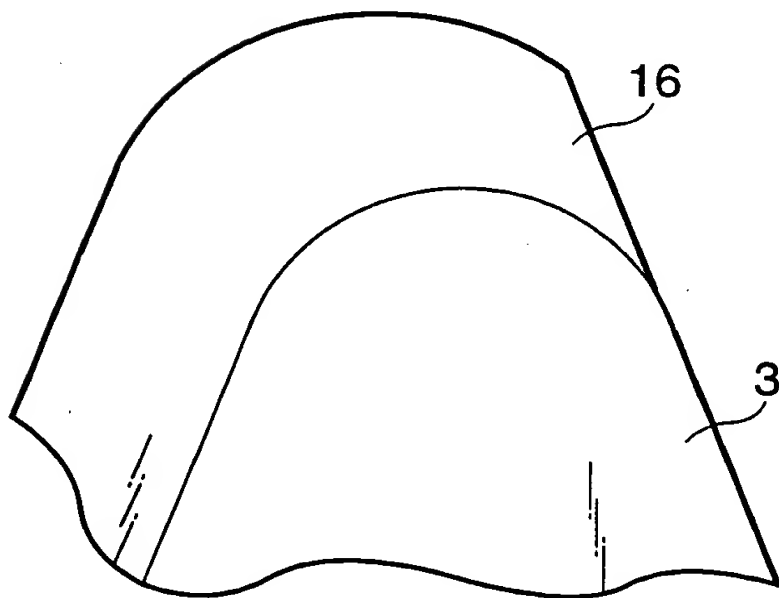


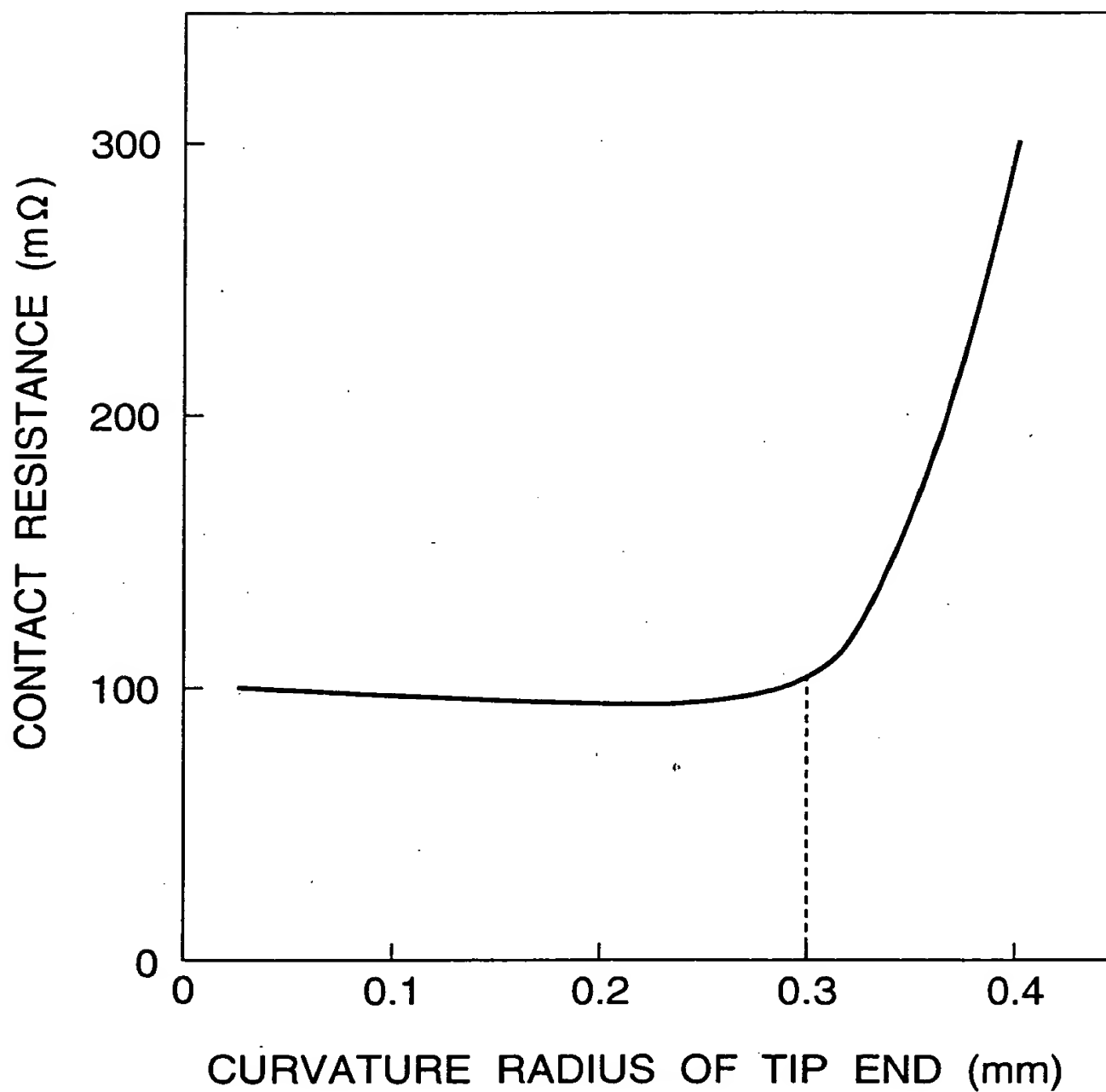
FIG.8



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FIG.9



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FIG.10

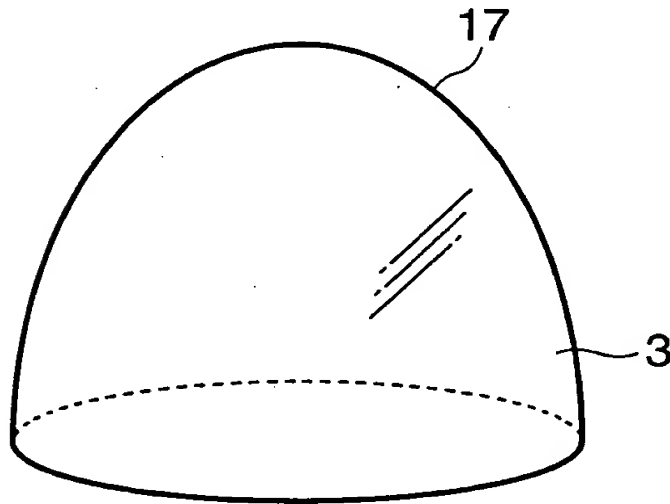
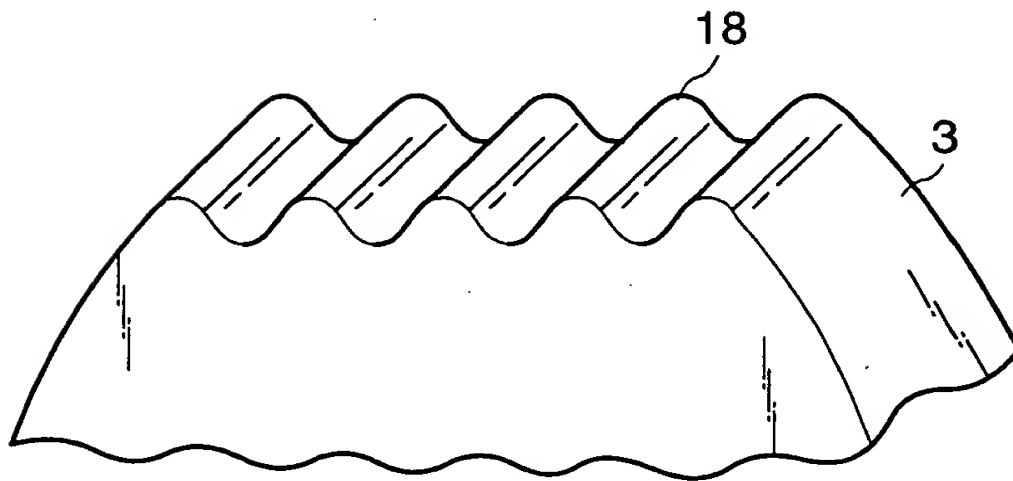


FIG.11





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FIG.12

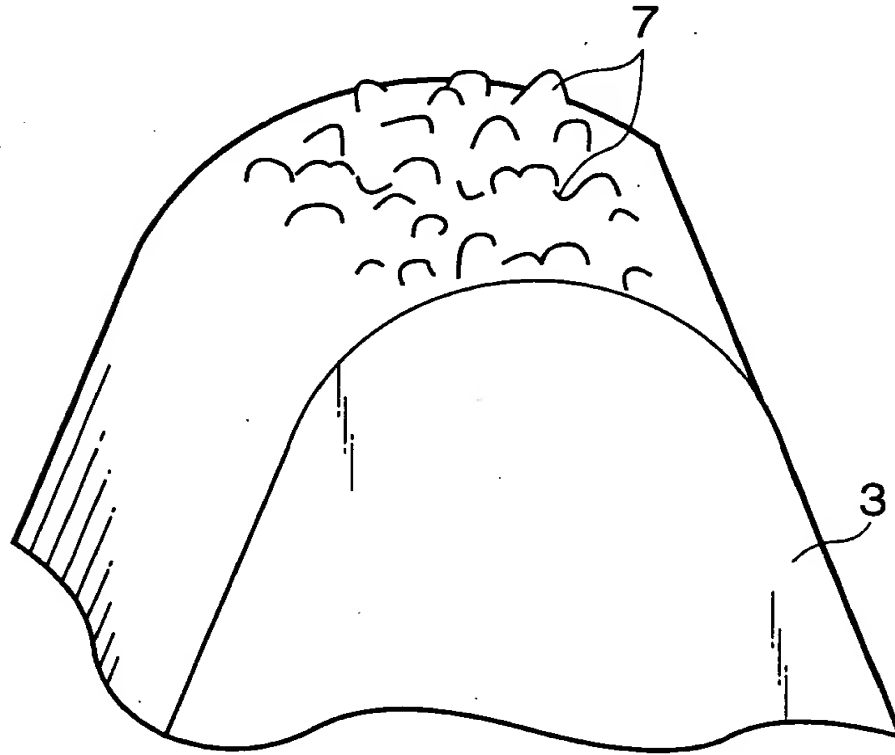
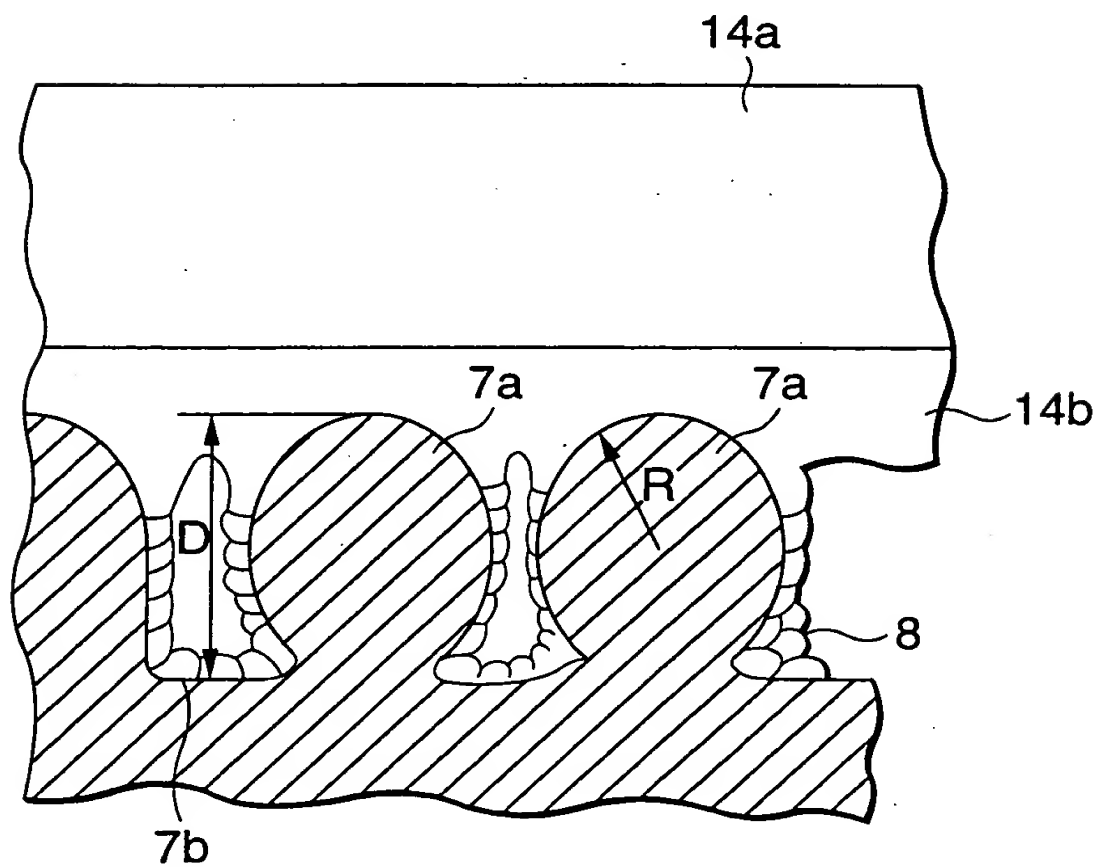


FIG.13





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FIG.14A

FIG.14B

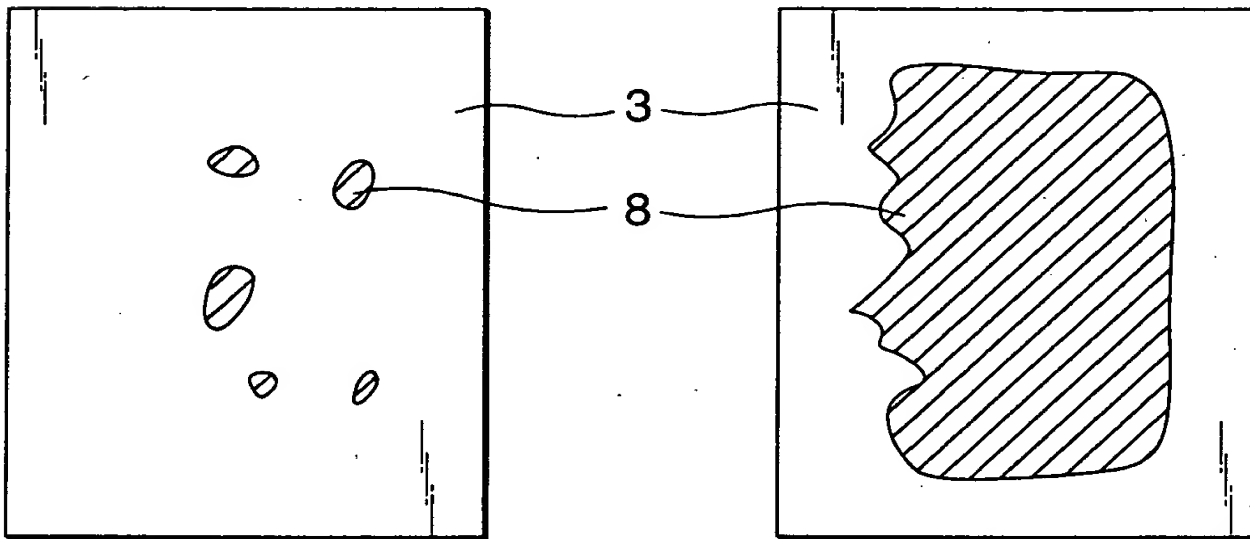
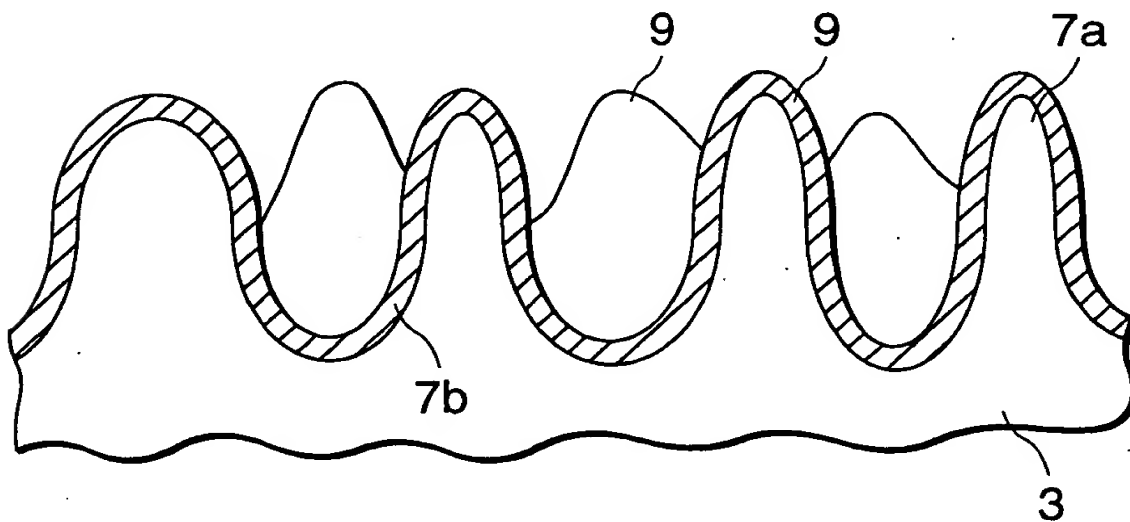


FIG.15





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FIG.16

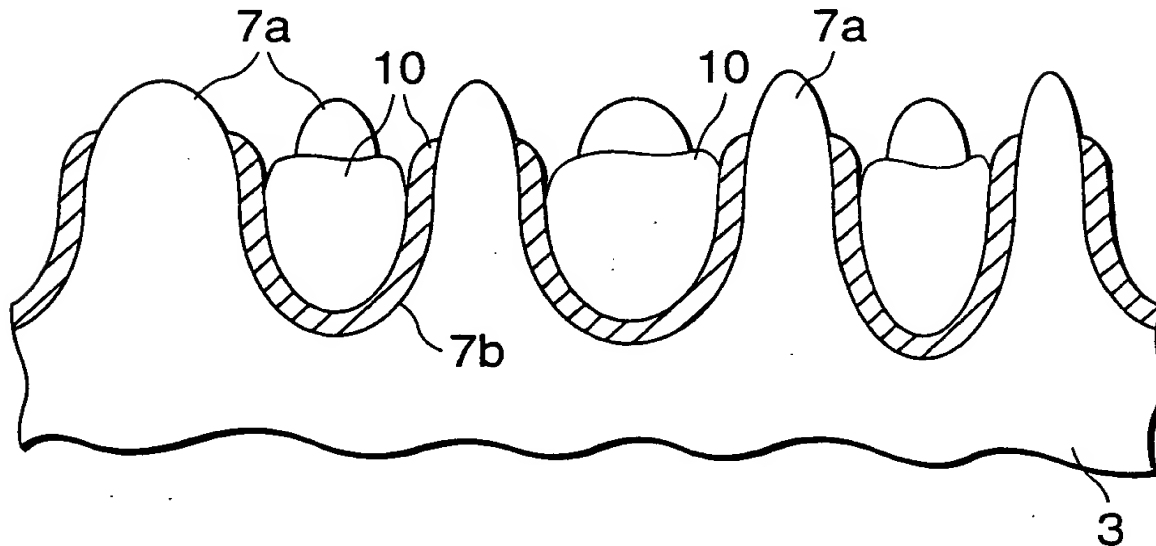
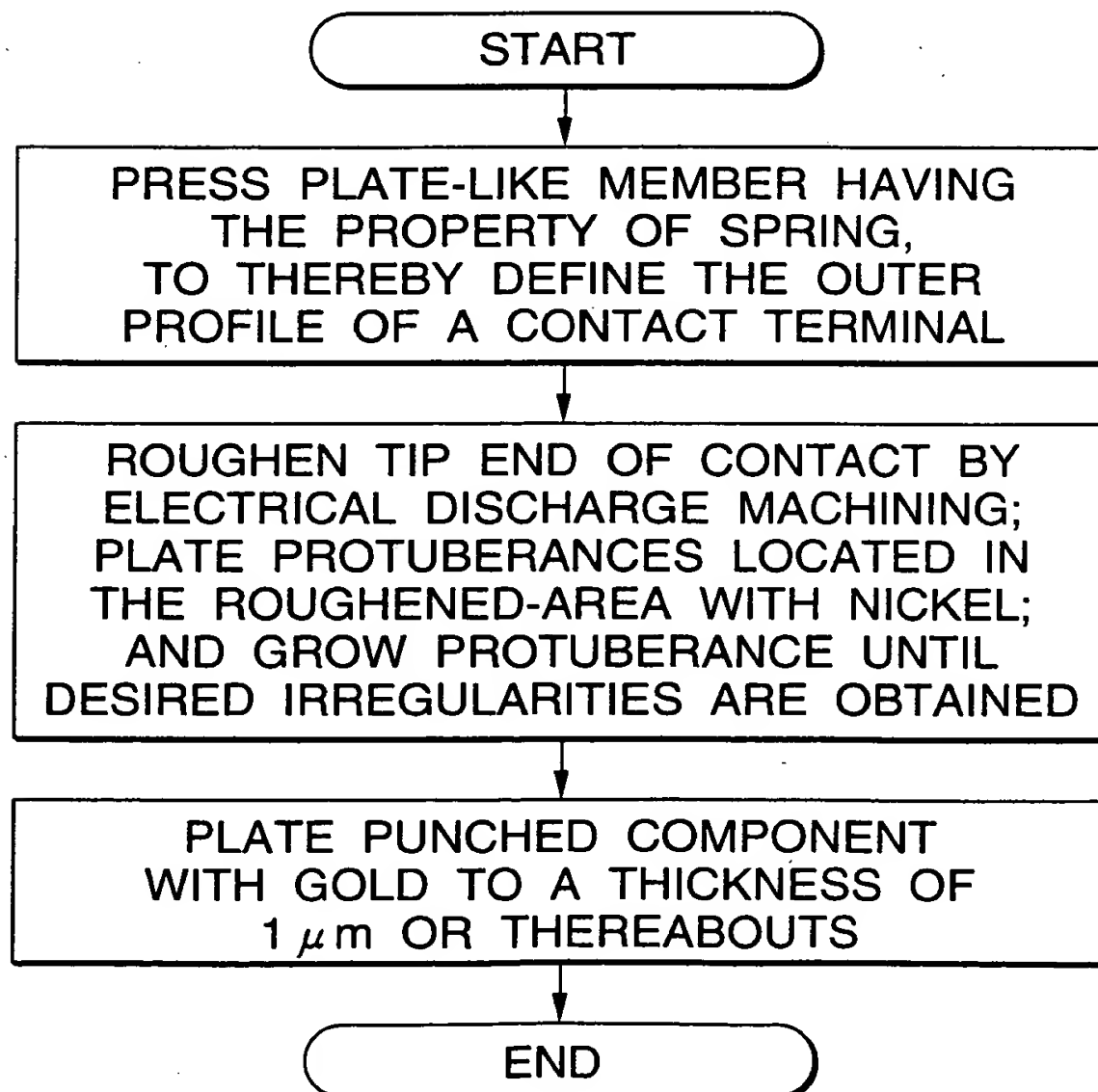


FIG.17



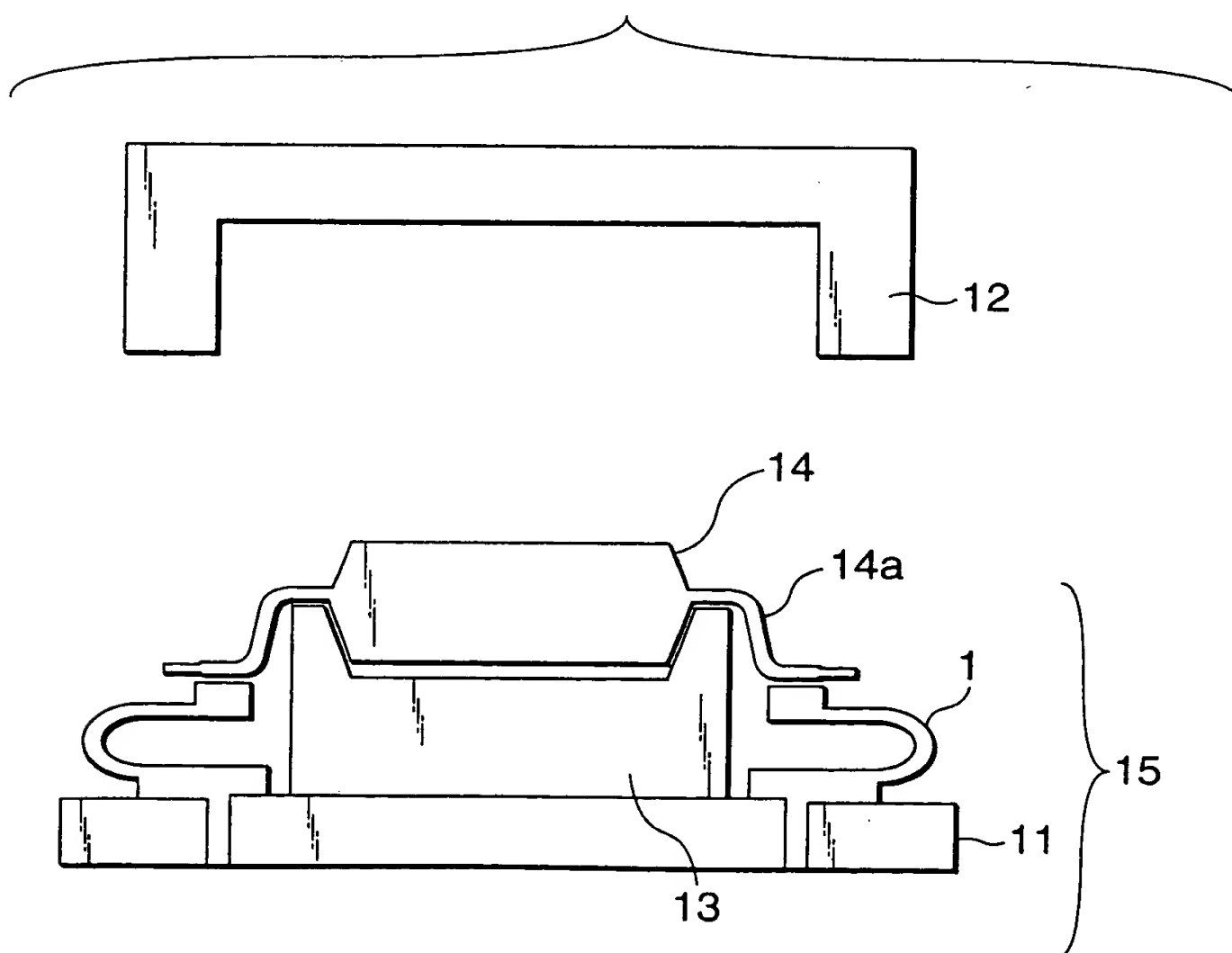


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FIG.18

	NUMBER OF LOADED ICs n	NUMBER OF DEFECTIVE ICs m	FRACTION DEFECTIVE m/n
CONTACT TERMINAL A	3016	12	0.4%
CONTACT TERMINAL B	3000	29	1.0%
CONTACT TERMINAL C	2900	61	2.1%

FIG.19 PRIOR ART



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FIG.20 PRIOR ART

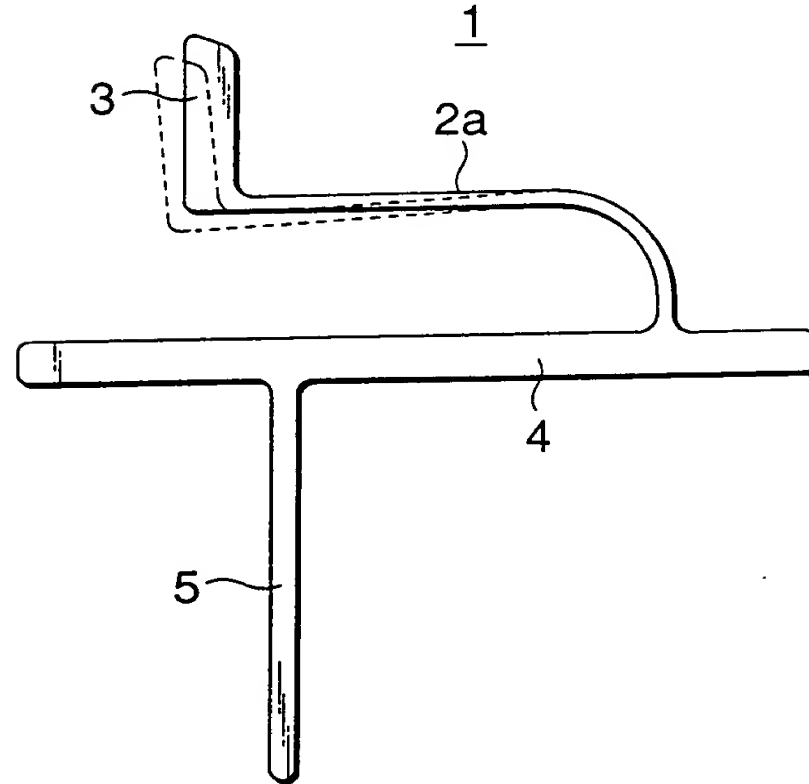


FIG.21 PRIOR ART

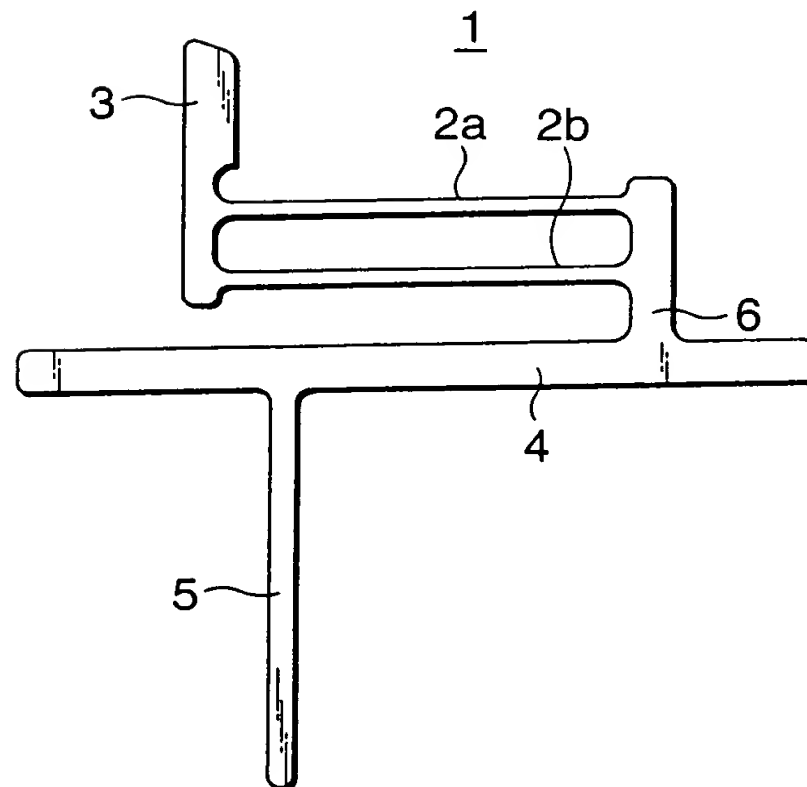




FIG.22 PRIOR ART

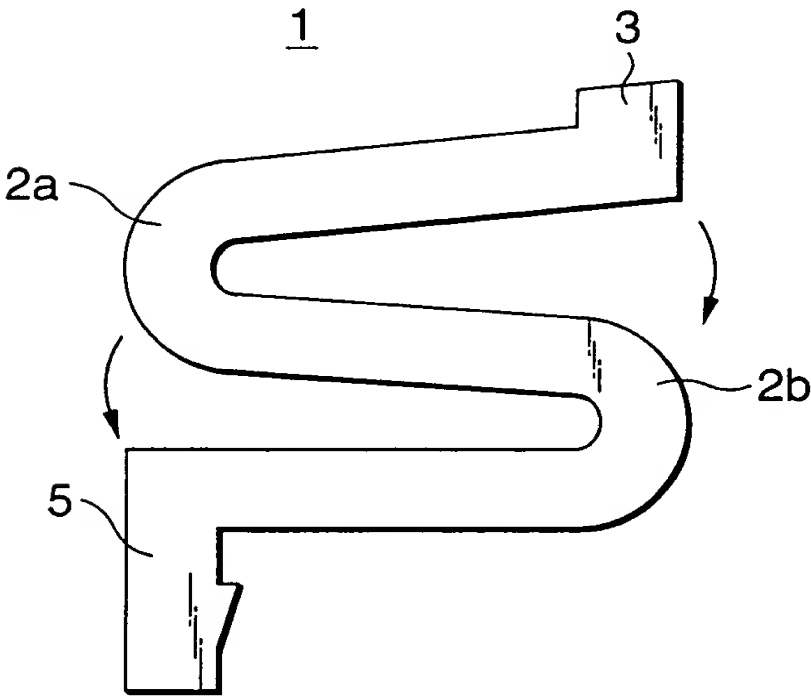
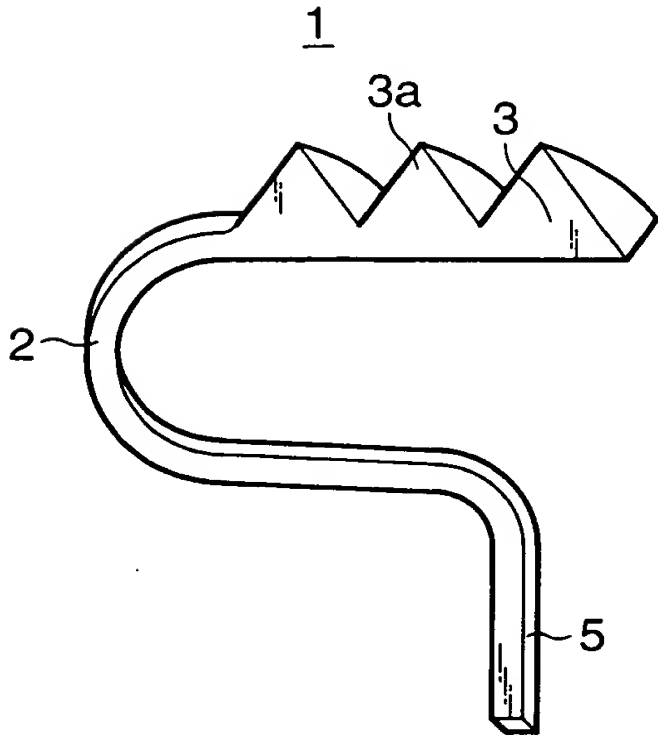


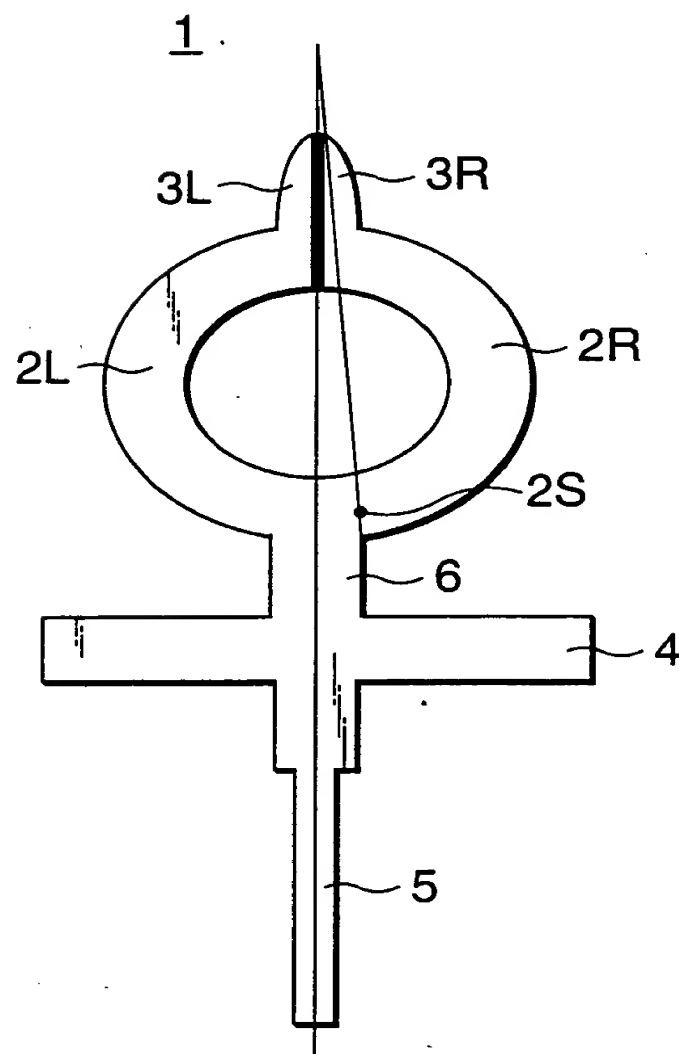
FIG.23 PRIOR ART



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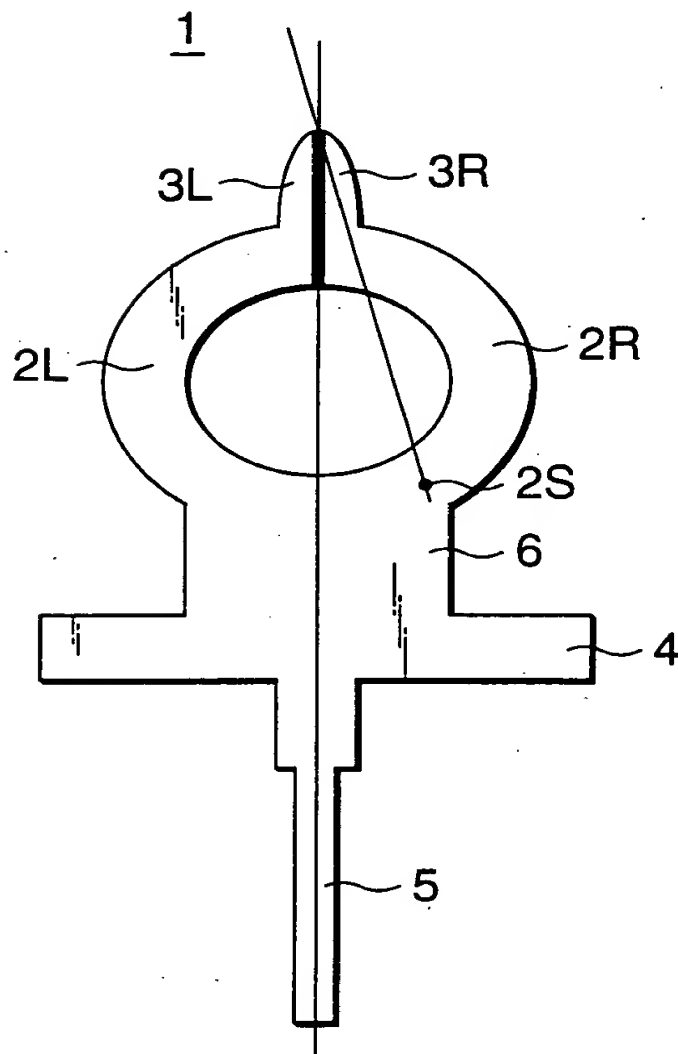
FIG.24



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FIG.25



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FIG.26A

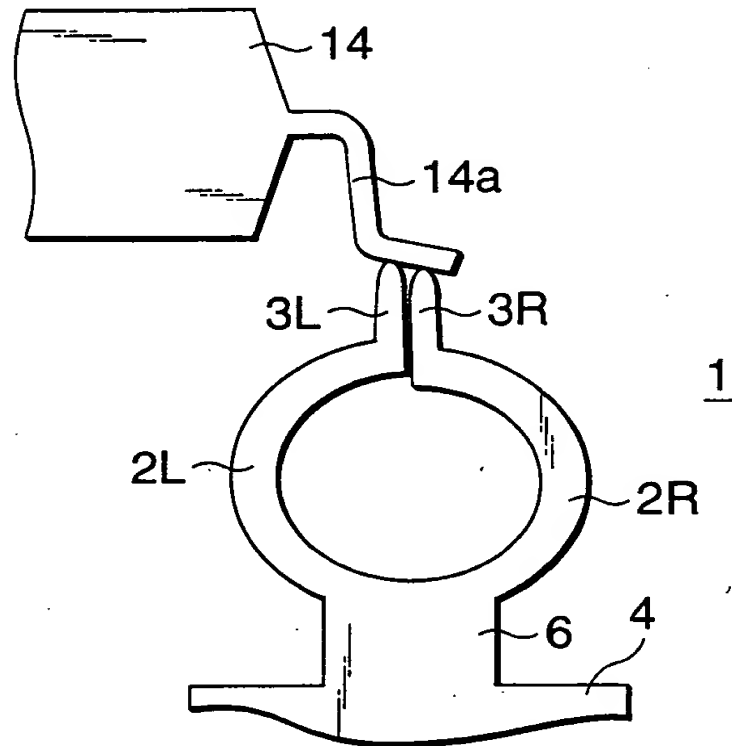
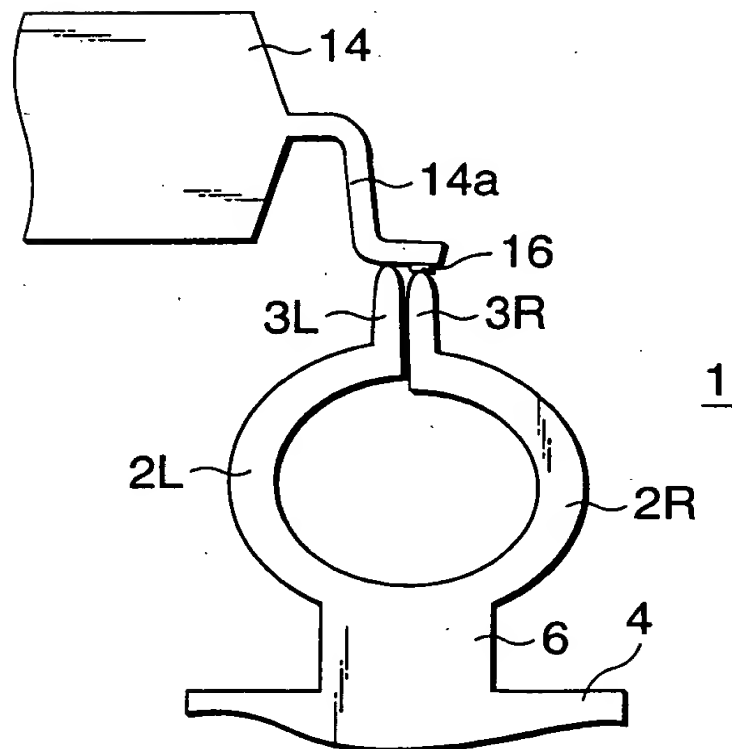


FIG.26B



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FIG.27

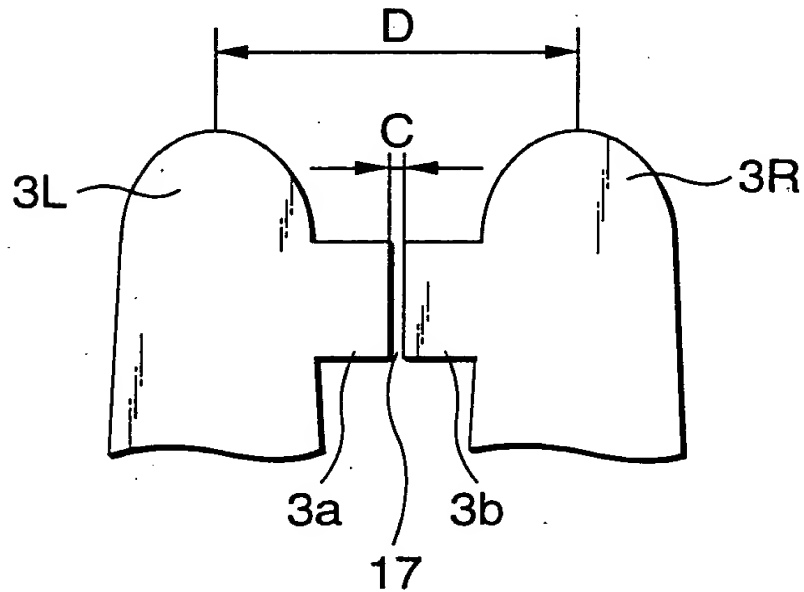
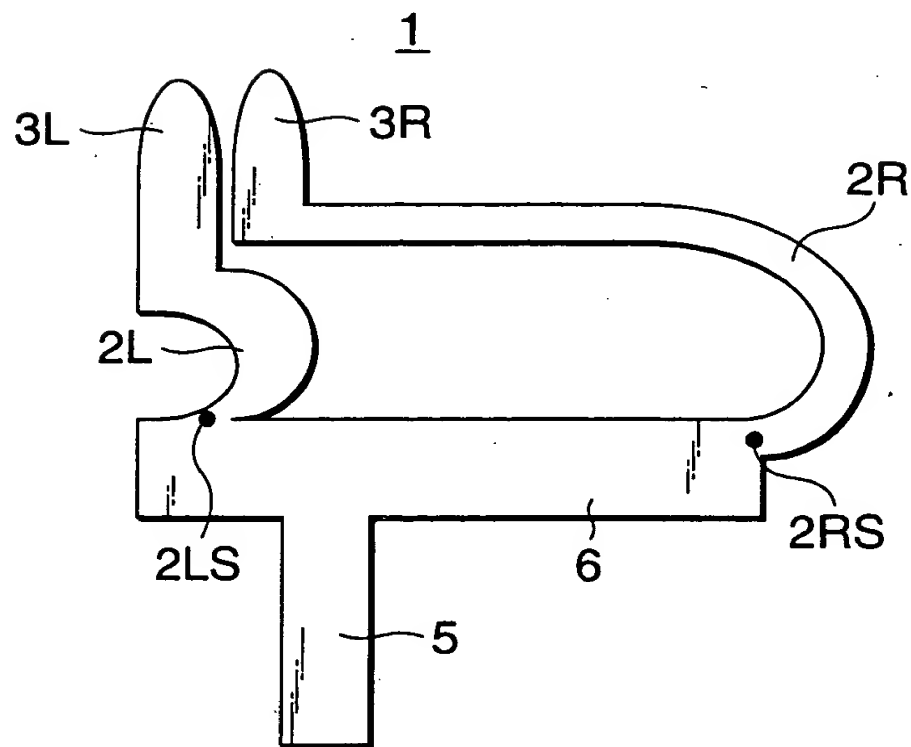


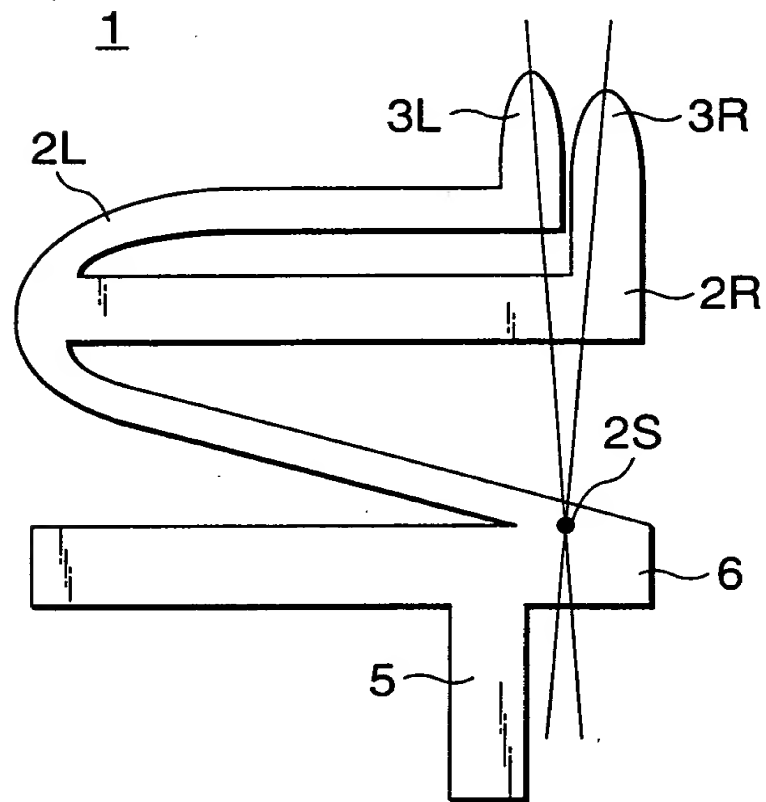
FIG.28



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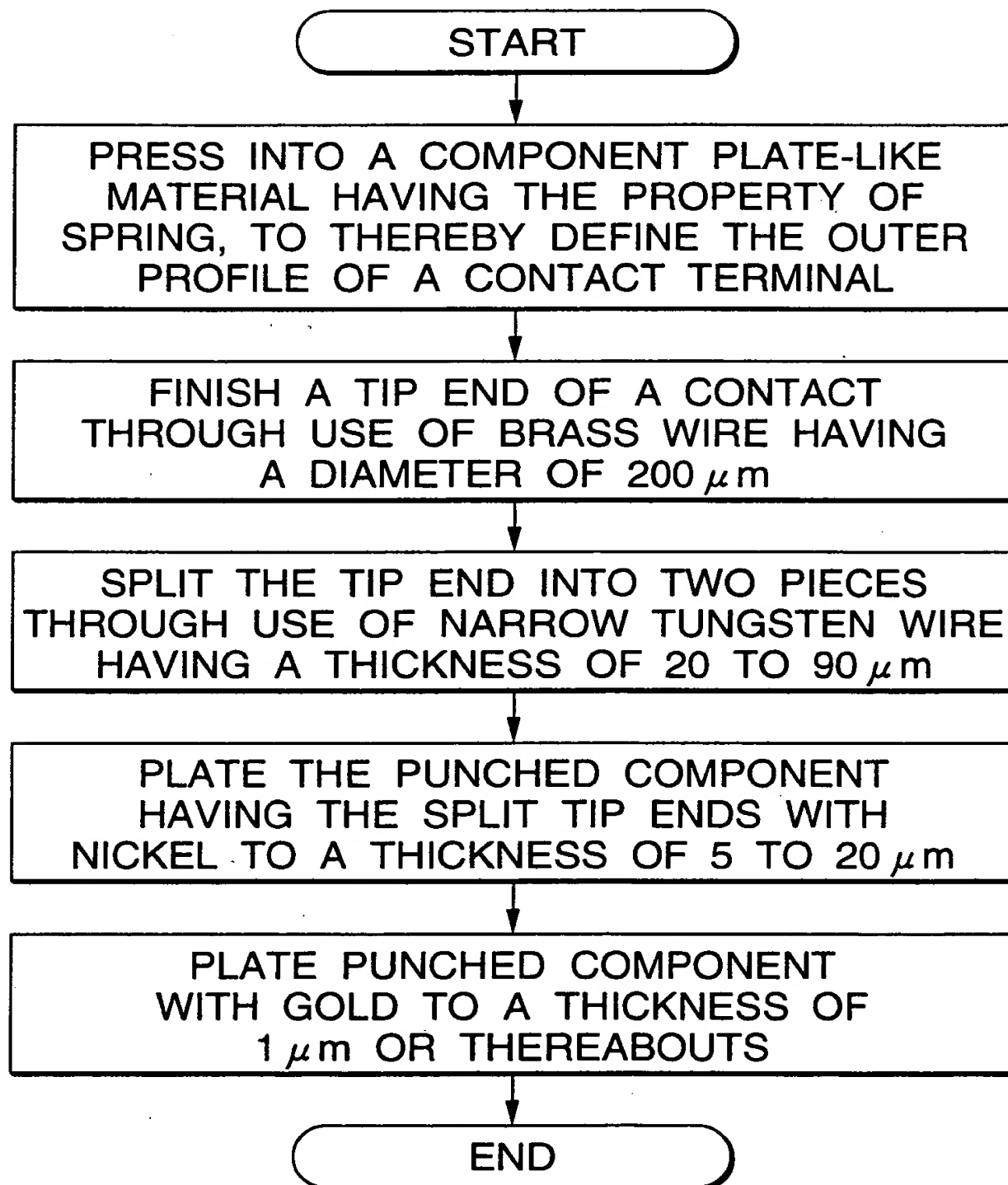
FIG.29



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FIG.30



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FIG.31

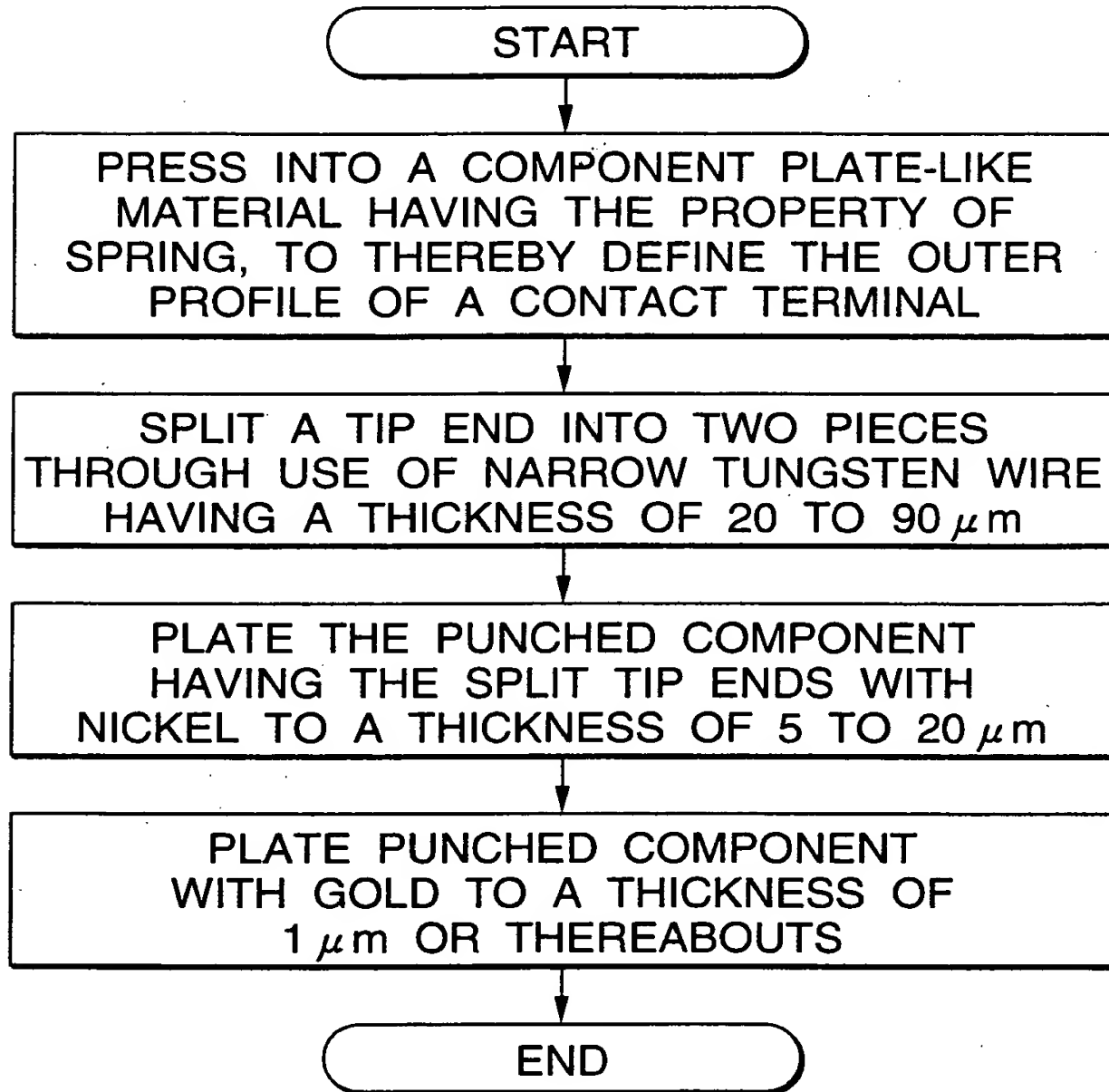


FIG.32

	NUMBER OF LOADED ICs n	NUMBER OF DEFECTIVE ICs m	FRACTION DEFECTIVE m/n
CONTACT TERMINAL A	3004	14	0.5%
CONTACT TERMINAL B	3005	10	0.3%
CONTACT TERMINAL C	3010	60	2.0%